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Brief Biographical Sketch

Laung-Terng (L.-T.) Wang, chairman and chief executive officer (CEO) of SynTest Technologies (Sunnyvale, CA), is also a visiting professor in the Department of Electrical Engineering at National Taiwan University, the Department of Creative Informatics at Kyushu Institute of Technology, and the School of Software at Tsinghua University. He received his BSEE and MSEE degrees from National Taiwan University in 1975 and 1977, respectively, and his MSEE and EE Ph.D. degrees under the Honors Cooperative Program (HCP) from Stanford University in 1982 and 1987, respectively. He worked at Intel (Santa Clara, CA) and Daisy Systems (Mountain View, CA) from 1980 to 1986 and was with the Department of Electrical Engineering of Stanford University as Research Associate and Lecturer from 1987 to 1991.

Encouraged by his advisor and professor Edward J. McCluskey, a member of the National Academy of Engineering, Dr. Wang founded SynTest Technologies in 1990. The design-for-testability (DFT) technologies Dr. Wang has developed have been successfully implemented in thousands of ASIC designs worldwide. He currently holds 25 U.S. Patents, 4 European Patents (each registered in Britain, Germany, and France), and one Chinese Patent in the areas of scan synthesis, test generation, at-speed scan testing, test compression, logic built-in self-test (BIST), and design for debug-and-diagnosis (DFD).

Dr. Wang spearheaded efforts on raising over $2 million to honor his undergraduate advisor and NTU chair professor Irving T. Ho (Stanford Ph.D., 1961), and his graduate advisor and Stanford professor Edward J. McCluskey (MIT ScD, 1956). Since 2003, he has helped establish a number of endowed chair professorships, graduate fellowships, and undergraduate scholarships at Stanford University, National Taiwan University, Tsinghua University, and Shanghai Jiao Tong University. He also co-authored and co-edited three internationally used DFT/EDA textbooks – *VLSI Test Principles and Architectures* (2006), *System-on-Chip Test Architectures* (2007), and *Electronic Design Automation* (2009) – with sales over 4,500 copies by December 2009.

A member of Sigma Xi, Dr. Wang received a 2007 Meritorious Service Award from the IEEE Computer Society and is a co-recipient of the 2008 IEICE Information and Systems Society Excellent Paper Award for an excellent series of papers that appeared in IEICE Transactions on Information and Systems during a period of five years. He is a Fellow of the IEEE, a Golden Core Member of the IEEE Computer Society, and serves on the 2010 IEEE Computer Society Fellow Evaluation Committee.

Selected Publications

[Books]

[1] **L.-T. Wang**, C.-W. Wu, and X. Wen, editors, *VLSI Test Principles and Architectures: Design for Testability*, (808 pages), Morgan Kaufmann, San Francisco, 2006.

[2] **L.-T. Wang**, C. E. Stroud, and N. A. Touba, editors, *System-on-Chip Test Architectures: Nanometer Design for Testability*, (896 pages), Morgan Kaufmann, San Francisco, 2007.

[3] **L.-T. Wang**, Y.-W. Chang, and K.-T. Cheng, editors, *Electronic Design Automation: Synthesis, Verification, and Test*, (976 pages), Morgan Kaufmann, San Francisco, 2009.

[Book Chapters]

[1] **L.-T. Wang**, X. Wen, and Khader S. Abdel-Hafez, *Design for Testability,* (67 pages), in Chapter 2, *VLSI Test Principles and Architectures: Design for Testability*, pp. 37-103, Morgan Kaufmann, San Francisco, 2006.

[2] **L.-T. Wang**, *Logic Built-In Self-Test,* (78 pages), in Chapter 5, *VLSI Test Principles and Architectures: Design for Testability*, pp. 263-340, Morgan Kaufmann, San Francisco, 2006.

[3] **L.-T. Wang**, editor, "Industry Practices" (13 pages), in *Test Compression*, co-authored by X. Li, K.-J. Lee, and N. A. Touba, in Chapter 6, *VLSI Test Principles and Architectures: Design for Testability*, pp. 376-388, Morgan Kaufmann, San Francisco, 2006.

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[5] N. A. Touba, **L.-T. Wang**, and C. E. Stroud, *Introduction,* (40 pages), in Chapter 1, *System-on-Chip Test Architectures: Nanometer Design for Testability*, pp. 1-40, Morgan Kaufmann, San Francisco, 2007.

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[7] **L.-T. Wang**, M. Nourani, and T.M. Mak, *Coping with Physical Failures, Soft Errors, and Reliability Issues,* (72 pages), in Chapter 10, *System-on-Chip Test Architectures: Nanometer Design for Testability*, pp. 351-422, Morgan Kaufmann, San Francisco, 2007.

[8] **L.-T. Wang**, C. E. Stroud, and K.-T. Cheng, *Logic Testing*, (13 pages), in *Encyclopedia of Computer Science and Engineering*, Vol. 3, pp. 1770-1782, B. W. Wah, editor, J. Wiley & Sons, Hoboken, NJ, 2009.

[9] C. E. Stroud, **L.-T. Wang**, and Y.-W. Chang, *Introduction,* (38 pages), in Chapter 1, *Electronic Design Automation: Synthesis, Verification, and Test*, pp. 1-38, Morgan Kaufmann, San Francisco, 2009.

[10] **L.-T. Wang**, *Design for Testability,* (76 pages), in Chapter 3, *Electronic Design Automation: Synthesis, Verification, and Test*, pp. 97-172, Morgan Kaufmann, San Francisco, 2009.

[11] **L.-T. Wang**, X. Wen, and S. Wu, *Test Synthesis*, (44 pages), in Chapter 7, *Electronic Design Automation: Synthesis, Verification, and Test*, pp. 405-448, Morgan Kaufmann, San Francisco, 2009.

[12] **L.-T. Wang** and C. E. Stroud, *Fundamentals of VLSI Testing*, (29 pages), in *Power-Aware Testing and Test Strategies for Low Power Devices*, pp. 1-29, P. Girard, N. Nicolici, and X. Wen, editors, Springer, Boston, 2009.

[Journal Papers]

[1] **L.-T. Wang** and E.J. McCluskey, "Condensed Linear Feedback Shift Register (LFSR) Testing – A Pseudoexhaustive Test Technique," *IEEE Transaction on Computers*, Vol. C-35, No. 4, pp. 367-370, April 1986.

[2] **L.-T. Wang** and E.J. McCluskey, "Linear Feedback Shift Register Design Using Cyclic Codes," *IEEE Transaction on Computers*, Vol. 37, No. 10, pp. 1302-1306, October 1987.

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[5] X. Wen, Y. Yamashita, S. Kajihara, **L.-T. Wang**, K.K. Saluja, and K. Kinoshita, "A New Method for Low-Capture-Power Test Generation for Scan Testing," *IEICE Trans. on Information and Systems,* Vol. E89-D, No. 5, pp. 1679-1686, May 2006. **(Excellent Paper Award)**

[6] X. Wen, S. Kajihara, K. Miyase, Y. Yamato, **L.-T. Wang**, K.K. Saluja, and K. Kinoshita, "A Per-Test Fault Diagnosis Method Based on the X-Fault Model," *IEICE Trans. on Information and Systems,* Vol. E89-D, No. 11, pp. 2756-2765, November 2006.

[7] X. Wen, S. Kajihara, K. Miyase, T. Suzuki, K. K. Saluja, **L.-T. Wang**, and K. Kinoshita, "A Novel ATPG Method for Capture Power Reduction During Scan Testing," *IEICE Trans. on Information and Systems,* Vol. E90-D, No. 9, pp. 1398-1405, September 2007. **(Excellent Paper Award)**

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[10] **L.-T. Wang**, X. Wen, S. Wu, H. Furukawa, H.-J. Chao, B. Sheu, J. Guo, and W.-B. Jone, "Using Launch-on-Capture for Testing BIST Designs Containing Synchronous and Asynchronous Clock Domains," *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 29, No. 2, pp. 299-312, February 2010.

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[1] **L.-T. Wang** and E.J. McCluskey, "Concurrent Built-In Logic Block Observer (CBILBO)," *Proc. IEEE 1986 Int'l Symposium on Circuits and Systems (ISCAS-1986)*, Vol. 3, pp. 1054-1057, May 1986.

[2] **L.-T. Wang**, N.E. Hoover, E.H. Porter, and J.J. Zasio, "SSIM: A Software Levelized Compiled-Code Simulator," *Proc. ACM/IEEE 1987 Design Automation Conference (DAC-1987)*, pp. 2-8, Miami Beach, Florida, June 28-July 1, 1987.

[3] **L.-T. Wang**, X. Wen, H. Furukawa, F.-S. Hsu, S.-H. Lin, S.-W. Tsai, K.S. Abdel-Hafez, and S. Wu, "VirtualScan: A New Compressed Scan Technology for Test Cost Reduction," *Proc. IEEE 2004 Int'l Test Conference (ITC-2004)*, pp. 916-925, Charlotte, NC, October 2004.

[4] X. Wen, Y. Yamashita, S. Kajihara, **L.-T. Wang**, K.K. Saluja, and K. Kinoshita, "On Low-Capture-Power Test Generation for Scan Testing," *Proc. IEEE 2005 VLSI Test Symposium (VTS-2005)*, pp. 264-270, Palm Spring, CA, May 2005.

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[8] S. Wu, **L.-T. Wang**, Z. Jiang, J. Song, B. Sheu, X. Wen, M. S. Hsiao, J. C.-M. Li, J.-L. Huang, and R. Apte, "On Optimizing Fault Coverage, Pattern Count, and ATPG Run Time Using A Hybrid Single-Capture Scheme for Testing Scan Designs," *Proc. IEEE 2008 Int'l Symposium on Defect and Fault Tolerance (DFT-2008)*, pp. 143–151, Cambridge, MA, October 2008.

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[10] **L.-T. Wang**, N. A. Touba, Z. Jiang, S. Wu, J.-L. Huang, and J. C.-M. Li, "CSER: BISER-Based Concurrent Soft-Error Resilience," *Proc. IEEE 2010 VLSI Test Symposium (VTS-2010)*, pp. 153-158, Santa Cruz, CA, April 2010.

[Chinese Articles]

(05/12/2010) NTU Newsletter「江山代有才人出—同學你想出國深造嗎？」(Also in 30 雜誌)

(04/21/2010) NTU Newsletter「江山代有才人出—同學你的貴人在哪裡？」(Also in 30 雜誌)

(03/10/2010) NTU Newsletter「臺灣高等教育的迷思系列—講座基金設立之迫切性」(Also in 遠見雜誌)